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Automatic Integrated Circuit Die Positioning in the Scanning Electron Microscope

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Summary: In scanning electron microscope (SEM)-based integrated circuit (IC) failure analysis, there is often a need for manual location of a prespecified failure site in several ICs. Such a procedure is both tedious and time consuming. This paper presents a new vision-based die positioning system that can automatically locate a specified failure site without the need for a high-accuracy specimen stage. Depending on the appearance of the desired failure site, the system applies either image registration or feature tracking to locate the site. Experiments performed on a variety of IC samples show that the system is able to locate the failure site accurately, even in the presence of unfavorable conditions such as IC sample rotation and repetitive IC patterns.

Key words: die positioning, scanning electron microscopy, registration, template matching, automation

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Introduction

The scanning electron microscope (SEM) is an important tool in integrated circuit (IC) failure analysis. Very often, the failure analyst uses the SEM to locate manually and to inspect a previously identified failure site over several batches of ICs to determine whether the failure was due to repeated process defects, weak spots, or otherwise. The problem is exacerbated by the fact that the failure analyst often does not have access to the design layout database, even for products produced within the same company.

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This manual process of locating the desired failure site is extremely tedious and time consuming because of several reasons. First, there is the limited field of view and image resolution of which the SEM is capable. This limitation slows down the failure site location process since the IC cannot be viewed in its entirety. Next, the failure analyst usually has to rely on distinctly recognizable features on the IC to maneuver the SEM stage to the required failure site. If the IC being studied is a memory device such as a dynamic random access memory (DRAM) sample, there are no distinguishable features on the IC to aid the user during navigation. To compound the problem, new generation ICs are increasingly complex, multilayer devices that reside over larger chip areas.

The direct solution to the die positioning problem is to make use of an accurate SEM stage with absolute positioning accuracy better than a fraction of the minimum IC feature size. The stage coordinates of the desired failure site can then be saved and recalled as needed. However, many motorized SEM stages have a positioning accuracy no better than ±1 to 2 μm. To improve accuracy, high-accuracy stages fitted with linear encoders or interferometers may be retrofitted into SEM specimen chambers; however, this is an expensive approach that would also restrict the use of the SEM for other failure analysis tasks. Another drawback of depending on a stage-based solution is that the principal axes of the stage must be aligned with those of the sample.

Another solution is to make use of computer-aided design (CAD) IC layouts that can be linked to an SEM stage navigation system. The SEM stage can be driven to the failure site using the layout coordinates. Such approaches, however, have been limited mainly to commercial electron beam testing systems (Thong 1993). Also, some previous work in this area (Rosolen and King 1998) makes use of image processing to locate the desired failure site. Reference images are captured and cross correlated with live SEM images to track a path back to the failure site.

A new automatic die positioning system for the SEM is proposed and developed in this paper. The system is designed to be robust with respect to problems such as sample rotation and repetitive IC patterns. Moreover, it does not require the use of a high-accuracy SEM stage and is adaptable to present and future generations of ICs.

System Overview

In designing the die positioning system, a few important specifications had to be met. First, the system must be robust with respect to IC sample rotation and scaling. If the SEM images captured from one IC sample are rotated or scaled with respect to images from another sample, the system must still be able to locate the desired failure site. Second, the system must be adaptable to present and future generations of ICs. Finally, the system must perform well without the use of a high-accuracy SEM stage or any modifications that restrict the use of the SEM for other activities.

Given the above specifications, it was eventually decided that a machine vision approach would be used for automatic die positioning in the system. Such a machine vision-based system can emulate what a human operator would do in practice and is able to meet the required specifications. This system can overcome the problem of IC sample rotation and scaling by using image processing techniques. In addition, a machine vision approach offers the flexibility of adapting to present and future generations of ICs. The software image processing techniques can be easily modified to accommodate IC samples of differing complexity, minimum feature size, or appearance. Also, the high accuracy of machine vision algorithms enables one to locate the desired failure site within a resolution of a few pixels. As such, the need for an expensive, high-precision SEM stage is eliminated. Moreover, installing software machine vision algorithms into existing SEMs is a simple task, since many SEMs are now linked to workstations or PCs. There is no need to modify the existing SEM hardware, which might restrict the use of the SEM for other activities.

It should be recognized that the system has its limitations. For example, if the movement of the SEM stage is jerky and erratic, a human operator would be unable to locate the desired failure site. Under such conditions, the die positioning system is unlikely to perform any better. Also, since the machine vision algorithms are implemented in software, system speed will suffer. However, this is becoming less of a problem with the advent of fast microprocessors. Image processing techniques such as the fast Fourier transform (FFT) can now be performed in real-time.

An overview of the new die positioning system is shown in Figure 1. The hardware used consists of a Hitachi S-4100 SEM (Hitachi Scientific Instruments, Mountain View, Calif., USA) connected to a DEC AlphaStation 500/400 (Compaq, Houston, Tex., USA). The workstation captures live video images from the SEM using a frame grabber card. In addition, the workstation also controls various SEM parameters, such as SEM magnification level, via a RS-232 communication link. This link also allows control of the SEM stage via a stage controller. The machine vision software is written in *C* and runs under the *X Windows* environment.

Algorithm Development

The automatic die positioning algorithm used by the system relies on machine vision. To understand how machine vision is applied here, it is useful to analyze what happens when a human operator manually positions a die at a particular failure site. The manual positioning technique used depends very much on the type of failure site being considered.

If the desired failure site contains unique and distinguishing features, the operator can recognize the site for what it is. For repeated location of the same site on several batches of ICs, the operator would locate a convenient reference point with unique and distinguishing features. An example would be a fiducial marker on the die. Next, the operator notes down the SEM stage coordinates and magnification level. The desired failure site is then located and the above process is repeated. With both sets of stage coordinates, the operator can now determine the position of the failure site relative to the specified reference point.

To locate the failure site on any subsequent IC sample, the operator must carefully and accurately position the stage at the reference point specified earlier. The correct SEM magnification level is also applied. Knowing the position of the failure site relative to this reference point, the operator can then translate the stage to the failure site. For this translation step, the operator must also take into account any rotational effects, since subsequent IC samples are likely to be rotated with respect to the original. At the failure site, the SEM magnification is again adjusted to the correct level so that the appropriate features can be viewed.

The machine vision approach adopted by the die positioning system follows the above corresponding actions carried out by a human operator. This is implemented using a rotation-scale-translation (RST) invariant image registration procedure. To train the system, the operator specifies a convenient reference point on a training IC sample and captures a reference point image. The stage coordinates and magnification settings are also stored. The failure site is then located manually and the above training procedure is repeated. A test IC sample is inserted and the operator guides the system to the reference point. An image registration procedure, based on template matching by phase correlation, is carried out to align the stage at this point precisely, as illustrated in Figure 2.

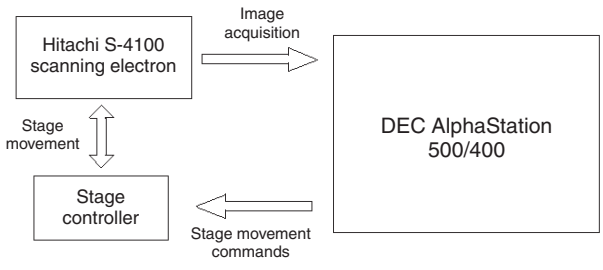

FIG. 1 Block diagram of the automatic die positioning system.

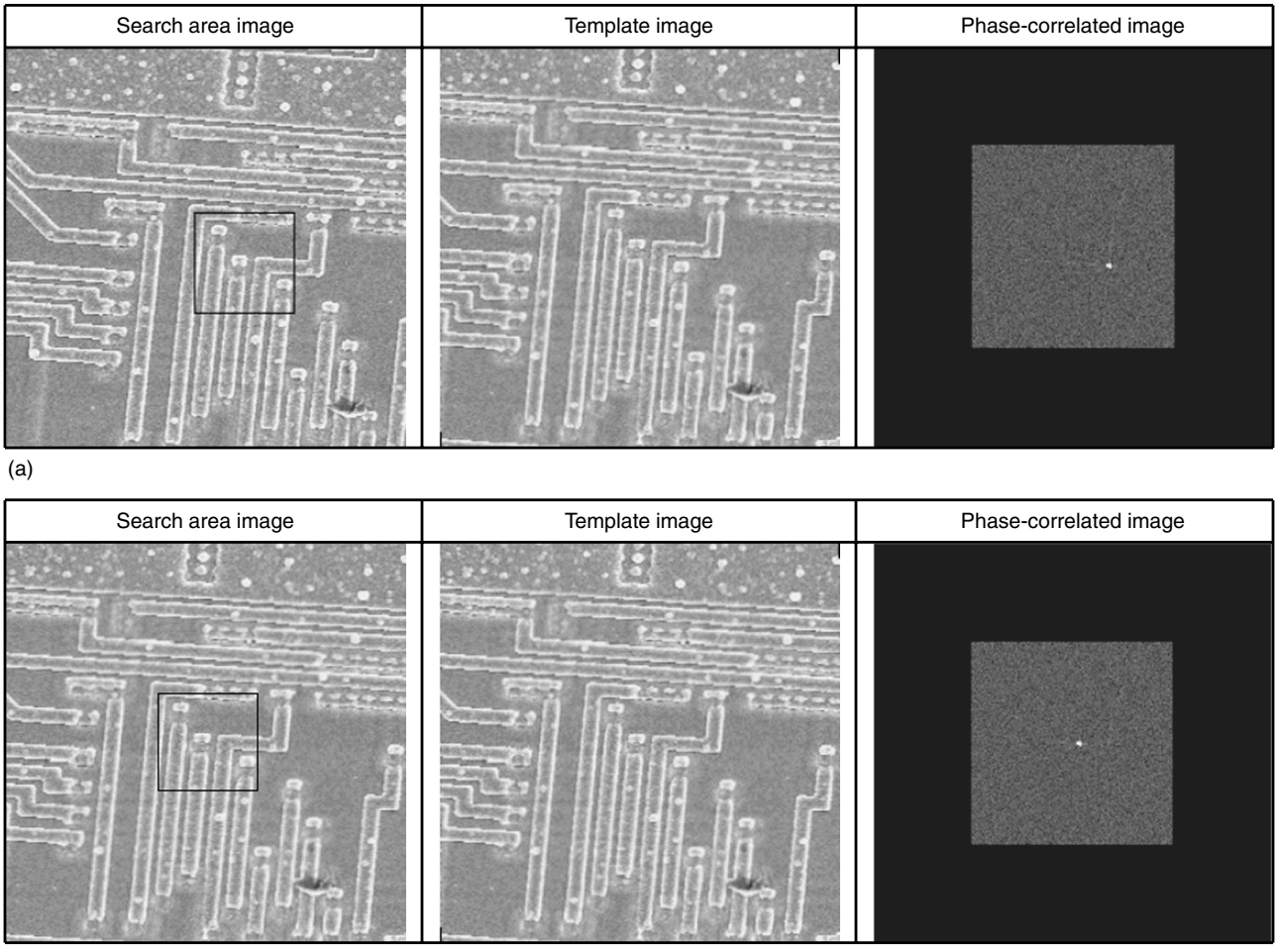

FIG. 2 Images illustrating the use of image registration to locate failure sites with unique features (horizontal field width = 126.1 μm). (a) Result of phase correlating two scanning electron microscope images differing by a translational offset. (b) Result of phase correlating the two images when they are precisely aligned.

If the desired failure site does not contain unique features, as is the case in many memory devices such as DRAM samples, a different approach must be adopted (Thong *et al*. 1999). Again, it is useful to consider what happens in a manual positioning procedure. Instead of relying on SEM stage coordinates, the failure analyst typically locates a failure site by manually counting individual memory cells (Fig. 3). This figure shows an example of a failure site taken from a 16 Mbit DRAM sample, containing many repetitive structures. Clearly, one cannot rely on SEM stage coordinates to reach this point since there are no unique and distinguishing features. The operator would not know whether the desired failure site has indeed been reached, or whether the stage was actually in a neighboring region.

The manual counting approach also makes use of a training IC sample. The operator first locates a convenient reference point with unique features. This might be the corner of a memory array. Next, the operator counts the cells as they pass out from the field of view (FOV) while the

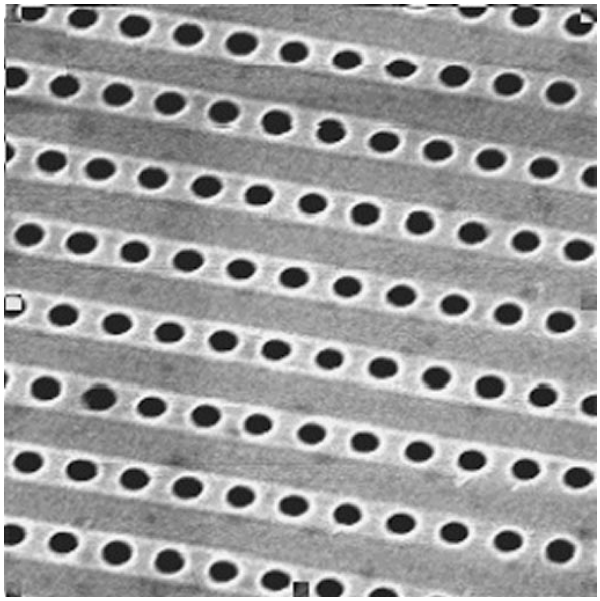

FIG. 3 Scanning electron microscope image of a failure site found on a 16 Mbit DRAM sample. Horizontal field width = 68.3 μm.

SEM stage is translated. This process involves visual tracking of a particular cell as it moves. When the cell passes out of the FOV, the operator has to focus on an adjacent cell and increase the number of cells counted. This continues until the desired cell is reached. On subsequent IC samples, the operator uses the cell count, determined earlier to reach the failure site. The reference point is first located and the cells are counted in a similar manner until the failure site is reached.

In the automatic die positioning system, the above manual positioning process is emulated by a feature-tracking strategy. To train the system, the user first specifies the reference point and captures a reference point image. Next, the failure site is then specified and the failure site image is captured. Following this, a series of template images is captured starting from the failure site back to the reference point. A test IC sample is then inserted and the user locates the previously specified reference point. Image registration is carried out to align the stage at the reference point precisely. The system training stage then terminates and the failure site location stage begins. Following this, template matching using the series of captured template images is carried out. By carefully monitoring the correlation peaks obtained, the system can track a path back to the desired failure site, as illustrated in Figure 4. This process of monitoring the correlation peaks mimics the counting strategy used by a human operator.

Implementation

Central to the automatic die positioning system is the implementation of an image registration procedure and a feature tracking solution. The former is used to locate failure sites with unique and distinguishable features, while the latter is used for failure sites with repetitive IC patterns.

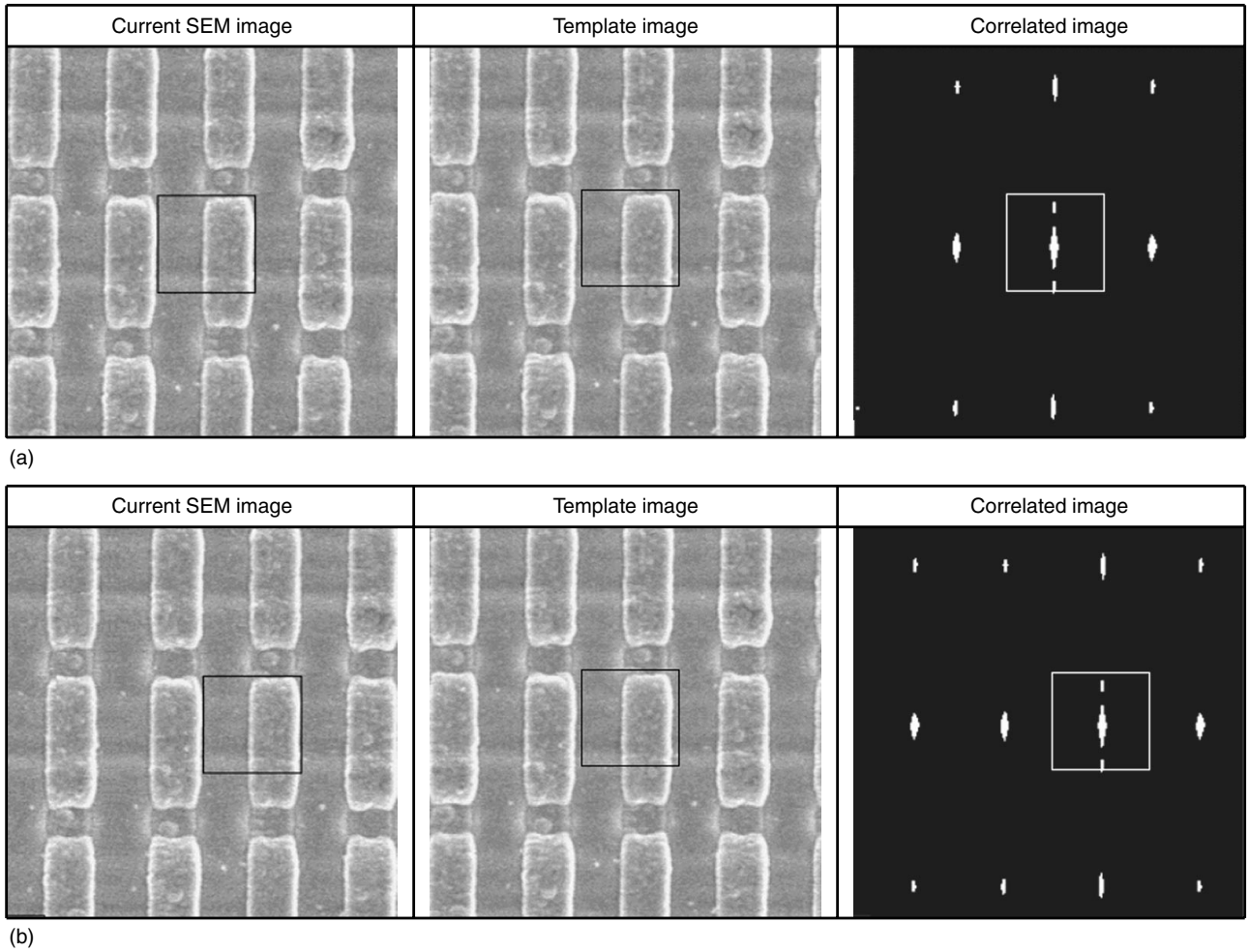

FIG. 4 Images illustrating the use of feature tracking to locate failure sites with repetitive integrated circuit patterns (horizontal field width = 44.6 μm). (a) Initial position of a correlation peak within the correlated image, when the two scanning electron microscope (SEM) images are in perfect alignment. (b) New position of the correlation peak when the current SEM image is translated slightly to the right.

These implementations are based on an image processing technique known as template matching (Brown 1992).

Template matching is defined as the process of locating the position of a subimage inside a larger image. The subimage is called the template and the larger image is called the search area. The template-matching process involves shifting the template over the search area and computing the similarity between the template and the window in the search area over which the template lies. The position where the largest similarity measure occurs is where the template is most likely to be located within the search area.

A commonly used similarity measure in template matching is the cross-correlation function or CCF (Lewis 1995). Formally, the CCF between the search area and the template is given by:

$$c(u,v) = \sum_{x=0}^{N-1}\sum_{y=0}^{N-1} f(x,y)t(x-u,y-v)$$

$$= f(x,y) \circ t(x,y) \tag{1}$$

where $f(x, y)$ is a given $M \times M$ search area image, $t(x, y)$ is a given $N \times N$ template image, $u = 0, 1, 2,\ldots, M - N$, and $v = 0, 1, 2,\ldots, M - N$. The CCF is a measure of the similarity between the search area and the template. A large cross-correlation value $c(u, v)$ at a certain shift position (u, v) indicates that the Euclidean distance between the template $t(x, y)$ and the search area $f(x, y)$ is minimized in this position, that is, the images are similar.

The above approach, known as template matching by cross correlation, is translation invariant but sensitive to changes in image intensity, image rotation, and image scaling. The first problem can be overcome by using phase-correlation (Kuglin and Hines 1975). This technique normalizes the transform coefficients prior to computing cross correlation in the frequency domain. This modifies Eq. (1) to become

$$\left(f(x,y) \circ t(x,y)\right)_{phase\ corr} = F^{-1}\left[\frac{|F(u,v)|^2 e^{-j2\pi(ux_o+vy_o)}}{|F^*(u,v)||F(u,v)|}\right]$$

$$= F^{-1}\left[e^{-j2\pi(ux_o+vy_o)}\right] \tag{2}$$

The term on the left hand side of Eq. (2) plays the role of a cross-correlation coefficient which indicates the strength of template matching at a particular shift position.

To correct for the effects of image rotation and scaling, the template matching procedure was modified. Progressive template matching by phase correlation is performed on the images being registered, to find the optimum rotational offset and scaling factor required to maximize the matching accuracy. These optimum values are searched for within a specified range and can be used to correct for any rotational and scaling offsets between the two images being matched (Caelli and Liu 1988). Standard template matching by phase-correlation can then be directly applied to find the translational offset between the images.

The above modified template matching technique is a rotation-scale-translation (RST) invariant procedure. It was incorporated into both the image registration procedure and the feature tracking solution. Experiments carried out have determined that the matching technique is very robust with respect to SEM image noise.

Results and Discussion

The system was first tested on an Intel 80486 DX-33 microprocessor die (Intel Corporation, Chandler, Ariz., USA) and a 12-bit analogue-to-digital converter (ADC). The fail-

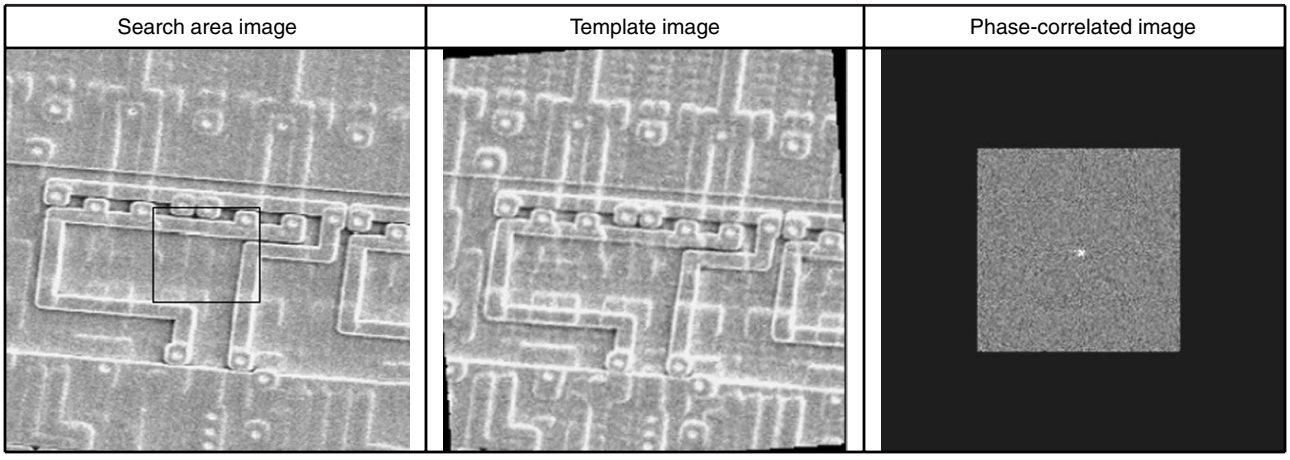

FIG. 5 Images obtained after the die positioning algorithm registers the current scanning electron microscopy image at the failure site of a microprocessor integrated circuit sample. Horizontal field width = 44.6 μm.

ure sites to be located on these samples were chosen so that they contained unique and distinguishing features. Experimental results show that the system can accurately locate the desired failure sites using an image registration procedure. This is true even under varying conditions of die orientation, complexity, and minimum feature size. The images in Figure 5 show the experimental results for the microprocessor sample.

The system was also tested on a region of repetitive IC patterns selected from an Intel 8087 arithmetic coprocessor sample. It was found that the feature-tracking approach implemented by the system was accurate provided the SEM stage step-size was limited to at most half the width of a repetitive pattern unit. The system would fail to differentiate between two regions of repetitive IC patterns if the stage step-size applied was too large.

The most computationally intensive process is the iterative search for the rotational offset between the two samples, taking typically 20 s on the current implementation platform. Frame-to-frame tracking including stage movement requires about 1 s to execute. The actual time taken to reposition the die will depend on the distance (number of frames) from the reference point.

Conclusions

A new automatic die positioning system has been developed for the SEM. The system makes use of machine vision to locate automatically a desired failure site on an IC sample. This is achieved without the use of a high-accuracy SEM stage or modifications to existing SEM hardware.

To locate failure sites containing unique features, such as those found on logic ICs, the system uses an image registration procedure. To locate failure sites containing repetitive IC patterns, such as those from DRAM samples, a feature-tracking approach is used. Experiments show that the system is able to locate failure sites accurately in a variety of different IC samples. The system is also flexible enough to be adapted for future generations of semiconductor devices.

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